IN THE SPECIFICATION:

Please amend the specification as follows:

Please replace the sentence beginning at page 7, line 16, with the following amended sentence:

- - This object [[is]] can be achieved by a test switching circuit having the features recited by the claims ~~of claim 1~~. - -

Please replace the sentence beginning at page 8, line 9, with the following amended sentence:

- - A further advantage of the test switching circuit according to the present invention having the features recited by the claims ~~of main claim 1~~ is that the data transmission in the normal operation mode is not affected, i.e. the parasitic capacitance is not increased by the test switching circuit according to the present invention. - -

Please replace the paragraph beginning at page 13, line 18, with the following amended paragraph:

- - As can be seen from figure 6 a high speed data interface **1** according to the present invention comprises an internal data input **2** and an internal data output **3** to connect the high speed data interface **1** to a data processing core **4A** within an integrated circuit. The integrated circuit comprises several high speed data interfaces

1. Each high speed data interface **1** has a transmission data output pad **4B** and a reception data input pad **5** to connect the integrated circuit to an external circuitry. A serial data stream is transmitted via the transmission output pad **4B** to the external circuit board and a serial data reception stream is received via the reception data pad **5**. In the embodiment as shown in figure 6 the high speed data interface **1** comprises a test signal generator **6** and a test signal analyzer **7** which are controlled by a mode control unit 8. In an alternative embodiment the test signal generator **6**, the test signal analyzer **7** and the mode control unit **8** are not provided within the high speed data interface **1** but separately within the integrated circuit. - -

Please replace the paragraph beginning at page 14, line 6, with the following amended paragraph:

- - In the data transmission signal path 17_1 a multiplexer **9** is provided with switches either data output by the data processing core **4A** or the test data pattern generated by the test signal generator **6** via an internal line **10** to a transmitter **11** which includes a serialiser and a pre-driving stage for signal amplification. The output of the transmitter **11** is connected via an internal line **12** to a final output driver stage **13** the output of which is connected via an internal line **14** to a programmable termination resistor stage **15**. The programmable termination resistor stage **15** is connected via an internal line **16** to the transmission data pad **4B** of the integrated circuit. The programmable termination resistor stage **15** comprises a plurality of

resistors which are switched by means of transistors to adapt the output impedance of the transmission signal path within the high speed data interface **1** to a load impedance connected to the transmission data pad **4B**. The transmitter **11**, the output signal driver **13** and the programmable termination resistor stage **15** form a transmission data signal path **17** within the high speed data interface **1**. - -

Please replace the paragraph beginning at page 16, line 11, with the following amended paragraph:

- - In a normal operation mode, the programmable termination resistor output stage **15** is separated from the programmable termination resistor input stage **18** by the test switching circuit **26**. The multiplexer **9** switches the data processing core **4A** of the integrated circuit to the data transmission signal path **17** and the demultiplexer **34** switches the output of the data reception signal path **25** to the data processing core **4A** of the integrated circuit. In the normal operation mode no test is performed and the data output by the core **4A** is transmitted via the transmission signal path **4B** to the external circuitry. In the same manner data received via the data reception pad **5** is forwarded by the data reception signal path **25** to the data processing core **4A** of the integrated circuit. - -

Please replace the paragraph beginning at page 17, line 35, with the following amended paragraph:

- - In a third operation mode, i.e. a receiver test mode, the test switching circuit **26** according to the present invention switches the data reception signal path **25** of the interface **1** to an internal test point. The test point **35** is connected in a preferred embodiment for a built in self test circuitry (BIST) forming a further test loop via the data processing core **4A** and the data reception signal path **25** of the high speed data interface **1**. In this receiver test mode it is possible to test the functionality of the data reception signal path **25** separately. - -

Please replace the paragraph beginning at page 20, line 34, with the following amended paragraph:

- - The test switching circuit **26** comprises six pairs of controllable switching transistors T1 to T6. In a preferred embodiment as shown in figure 7, the switching transistors are formed by MOSFET transistors. The first pair of switching transistors **TP1**, **TN1** (T1) is controlled by a first configuration bit **C1** of the configuration register **29** and switches the termination resistor output stage **15** to nodes **47-N**, **47-P** within the switching circuit **26** when the control bit **C1** is high. In the same manner, the sixth pair of switching transistors **TN6**, **TP6** (T6) switch the input **28-N**, **28-P** to the termination resistor input stage **18** to nodes **48-P**, **48-N** when the corresponding control bit **C6** is logical high. - -

Please replace the sentence beginning at page 21, line 11, with the following amended sentence:

- - The gates of the second pair of transistors **TN2**, **TP2** (T2) receive the control bit **C2** of the configuration bit and switches nodes **47-P**, **47-N** to a reference potential **GND-P**, **GND-N** if the configuration bit **C2** is logical high. - -

Please replace the paragraph beginning at page 21, line 16, with the following amended paragraph:

- - The gates of the third pair of transistors **TN3**, **TP3** (T3) receive a third configuration bit **C3** of the configuration register **29**. If the configuration of **C3** is high the transistors **TP3**, **TN3** (T3) connect the nodes **48-P**, **48-N** to **GNDP** and **GNDN**. - -

Please replace the paragraph beginning at page 21, line 22, with the following amended paragraph:

- - The gates of fourth pairs of transistors **TP4**, **TN4** (T4) receive a fourth configuration bit **C4**. In case that the fourth control configuration bit **C4** is logical high nodes **47-P**, **47-N** are connected to test point nodes **35-N**, **35-P**. - -

Please replace the sentence beginning at page 21, line 28, with the following amended sentence:

- - A fifth pair of transistors **TN5**, **TP5** (T5) is controlled by a fifth configuration bit (5) of the configuration register **29** and connects the test points **35-N**, **35-P** to nodes **48-P**, **48-N** when the fifth configuration bit **C5** is logical high. - -

Please replace the Abstract beginning at page 30, line 3, with the following amended Abstract:

- - A test switching circuit for a high speed data interface is disclosed. Test switching circuit for a high speed data interface [[(1)]] of an integrated circuit comprising switching transistors ~~(T1-T6)~~ which switch in a test mode a termination resistor output stage [[(15)]] of a data transmission signal path [[(17)]] to a termination resistor input stage [[(18)]] of a data reception signal path [[(25)]] to form an internal feedback test loop within said integrated circuit. - -

Please delete the phrase "(Figure 6)" at page 30, line 12, of the Abstract.